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Crystallographic Modification of Hard mask Properties

Abstract

A hardmask layer in the back end of an integrated circuit is formed from TaN having a composition of less than 50% Ta and a resistivity greater than 400 μOhm-cm, so that it is substantially transparent in the visible and permits visual alignment of upper and lower alignment marks through the hardmask and intervening layer(s) of ILD. A preferred method of formation of the hardmask is by sputter deposition of Ta in an ambient containing N_2 and a flow rate such that (N_2 flow)/(N_2 + carrier flow) > 0.5.